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Ultra High Frequency Baud rate data transfer speed(Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Data T/s) General Data and PRBS Data Serialize De-Serialize ASIC /SOC Array card Design using FDSOI Technology for Ultra high Speed long distance 6th sense space/satellite Wireless communication Engineering Smart computing products/Applications

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Abstract: *The Ambition is to HDL RTL Design & Verification for "Ultra High Frequency baud rate Data transfer speed (Tera, Peta, Exa, Zetta ,Yotta ,Xona ,Weka Hertz Data transfer/Seconds) General Data Serialize and De-serialize ASIC /SOC Array Card design of Different Data Stream Lengths (32,64, 128, 256 bit) and PRBS Data Serialize and De serialize of Various Different PRBS Tapped Seed word patterns- ($2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1,$2e^{52,}$-1, $2e^{63,}$-1) for ultra high Speed Long Distance 6th Sense Space/Satellite Wireless Data Serialize De-Serialize Communication Smart Computing Products".The Back End technology of this design by using FDSOI(Fully Depleted Silicon On Insulator Planar process technology very low power consumption for 6th Sense Wireless Communication Products. The 32,64,128,256 Data stream bit width based Data serialize and De-serialize done parallel. The Serialize module consists Parallel to Serial converter and De-serialize module consists of Serial to parallel Converter of Different Data bit lengths (32, 64,128,256 bit) and communication via wireless channel or vice versa did PRBS Data serialize De-Serialize ASIC. RTL Design & test bench software Programming Done by Verilog/System Verilog, Design Simulation and Synthesis, Verification done with Leading EDA Software design Tools. This Product Developed and suited for Ultra High Speed Wireless Serial Data Communication Products like Long distance Space/Satellite Data Communication, NOC-Network On Chip Routers, Data Bus Communication Interface Applications, Cloud Internet Computing Networks. All these Data Serialize De-Serialize ASIC /SOC Array Card are purely Synchronized with the Tera, Peta, Exa, Zetta, Yotta, Xona, Weka hertz Clock Frequency Standards. Why because this is newly invented product from existing products developed by Various reputed major IT Semiconductor/EDA Software MNC's /Corporate in terms Giga Hertz Clock Synchronized and Data transfer rate.*

Materials and Methods: *Data serialize De-Serialize Pseudo random seed word pattern methods of different PRBS $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 tapped sequence Elements and All these PRBS are purely synchronized with Ultra high clock frequency(MHz, GHz, THz, PHz, EHz, ZHz, YHz, XHz, WHz). The Soft IP Core Designed by System Verilog HDL/ Verilog HDL method. RTL Design Simulation done by Synopsys VCS 2020.1 software and Altera Model-Sim Software and Logic Design Flow & Synthesis done by Xilinx ISE and Altera Quartus EDA Tool Materials.*

Results: *Generation of Simulation Display and waveform for Ultra High Clock frequency(MHz, GHz, THz, PHz, EHz, ZHz, YHz, XHz, WHz) Synchronized Pseudo Random Binary Sequence (PRBS) Data serialize De-Serialize ASIC for efficient and effective High Quality Wireless High Serial Data transmission and Reception of*

Various different PRBS patterns$2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 NRZ of Ultra high speed Long distance wireless engineering Serial communication Applications/ products.

Keywords: *EDA – Electronic Design Automation, ASIC – Application Specific Integrated Circuit, SOC- System on Chip ,RTL – Register Transfer Level, PRBS- Pseudo Random Binary sequence, HDL- Hardware Description Language, FDSOI-Fully Depleted Silicon On Insulator, ISE- Integrated Software Environment, NRZ- Non return to Zero, NOC- Network on Chip Router. SER-DE-SER- Serialize De-Serialize.*

Date of Submission: 15-09-2022 Date of Acceptance: 30-09-2022

I. Introduction

In Modern Hi-Tech ASIC /SOC Communication & Information Technology World, So many Hi speed Serial **Communication Buses and Peripheral Bus Communication Interfaces, Interface cards, Internet on things, Wi-Fi Routers, NOC's, LTE ASIC** came to the market with **High Speed Data Rates** and **Band width** in terms of Mega & Giga bits per second . Data Transmission and Reception is in the form of Serial Format for very long Distance Communication. For this purpose, Data Serializes and De-Serializes are mainly used for conversion of High Speed Parallel to Serial and Serial to Parallel Communication Data Transmission & Reception Done through Wireless Serial Communication Link. Now We Designed Newly Invented Ultra High Frequency baud rate Data transfer speed (Tera, Peta, Exa, Zetta ,Yotta ,Xona ,Weka Hertz Data transfer/Seconds) Data Serialize and De-serialize ASIC /SOC Array Card Design of Different Data Stream Lengths (32,64, 128, 256 bit) at baud rate of Tera Bits Per Second(Tbps),Peta Bits Per Second(Pbps), Exa Bits Per Second(Ebps) , Zetta Bits Per Second(Zbps),Yotta Bits Per Second(Ybps), Xona Bits Per Second(Xbps), Weka Bits per Second(Wbps**)** by Synchronizing the Clock frequency Tera Hertz, Peta Hertz, Exa Hertz, Zetta Hertz, Yotta Hertz, Xona Hertz, Weka Hertz British Standard frequencies.

SERIAL TO PARALLEL ANALOGY

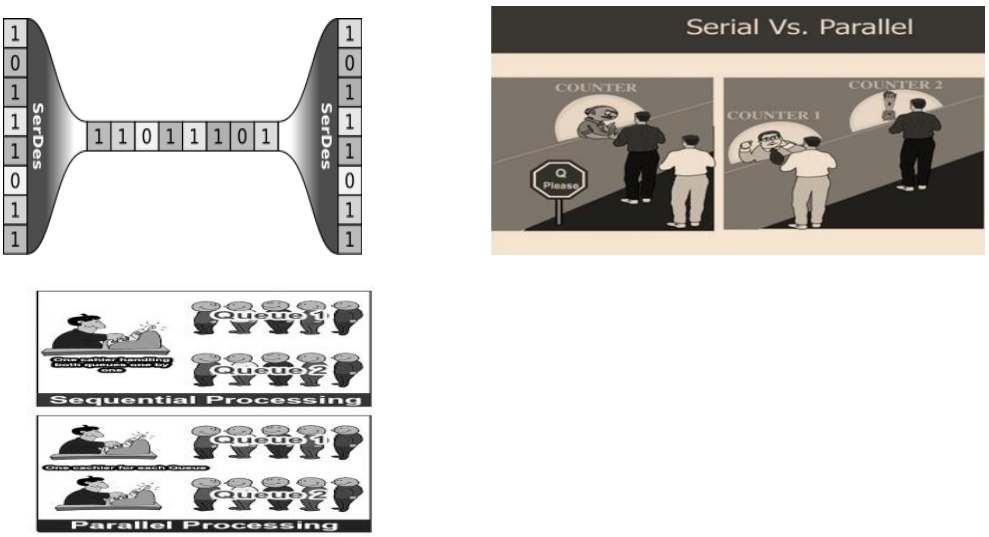

Fig.1 . Flight booking system serial/parallel queue Real time Analogy

The Above Analogy represents comparison of Serial and Parallel Analogy, for example an flight booking system, everybody maintained queue in sequential fashion, if we have one booking and more number of serial queues , then the counter is very difficult to issue the tickets to each guy in serial flow , it takes more time , whereas if we have more than one booking count mean sufficient number of counters w.r.t multiple serial queue, then , bookings issue tickets to each parallel at a time, so it is more flexible to issue tickets at a time, so parallel processing is much more faster than . similarly by comparison of this analogy , the parallel data

processing are much more faster than serial processing. Due to that, we are using Serialize De-serialize to convert the different data bits transfer from parallel to serial and serial to parallel conversion.

In Modern VLSI Technology Trends Speed, Power, Performance, Size (Complexity) are the major Constraint Factors for Designing High Quality VLSI Communication Chip Design IP Cores for Processing & Controlling High Speed Communication Data (Carrier and Base Band Signal) Information. Due to these, We Designed **Ultra High Frequency Baud rate data transfer speed(Tera,Peta,Exa,Zetta,Yotta,Xona,Weka Hertz Data T/s) Data Serialize De-Serialize ASIC /SOC Array Card Design** for Reliable Transmission & Reception through Wireless Serial Data Communication Link Layer. Now a Days Serial Communication is more popular compared to Parallel Communication w.r.t Latest Technologies & Products, Speed wise also almost Similar level compared to Parallel communication w.r.t Latest Data Serializers & Deserializers. But Parallel Communication always faster than Serial Communication. The LVDS Data Serializers & De-Serializers are mainly used in Hi-speed Data Bus Communication Protocol Interface Cards, Data Acquisition Cards & Equipment's like PCI Data Acquisition Interface Cards (Mbps, Gbps, etc) ,Internet based Wi-Fi Routers, Network Interface Cards , Network On Chip , Advanced High Speed MODEMs/ CODECs ,Central Data Computing Stations(Cloud Computing) of Big Software Blue Chip MNC's & Corporate etc. Data Serializers & De-Serializers are more compatible and Flexible. The High Speed Data Serialize Contains 32,64,128,256 data stream bit Parallel to Serial Converter, these Parallel Data Frames are converted Serial Data paths and Data De-Serializes Contains these 32,64,128,256 data bit Serial to Parallel Data (64 bit) Converters to get original Parallel Data or vice versa.

This High Speed Multi Channel Data Serializers & Deserializers contains Different Multi Channels. Each Channel has Different Data Transmission & Reception Rate in terms of Mega Bytes, Giga Bytes, Tera Bytes, Peta, Exa, Zetta, Yotta, Xona, Weka bytes per Second. These are mainly used in Space/Satellite Long Distance communication transmission and reception and Long Distance Communication links (LTE) in terms multiple thousands of Kilo Meters for Smart Computing System Products like Portable Multimedia Mobile Phones, I-Phones , Cellular Mobile Phones, Tablets , EEPADs etc. Data Serialize and De Serialize Contains Transmitter & Receiver on both sides (Transmitter & Receiver). Data Serialize and De Serialize contains Electrical Routing Switches Like Multiplexers, De-Multiplexers for Routing of Data Frames Transmission and Receptions of Different Channels. Serial Communication Link Shifts Data Serially from transmitter to Receiver Side. The next generation of IC Product uses size in-terms of nanometers 10, 25, 45, 65 nm to integrate more logic functions, so that higher performance, speed logic density achieved also significantly reduces number of routing paths, interconnections between blocks. The key constraints are increasing demand of bandwidth is that we use more faster high speed serial communication links and transceivers , framers & deframers. Data links with transceivers supports higher data throughput, more power efficient and higher system integration.

A high-speed serial link starts with low-frequency parallel data sampled by a synthesized clock and serialized into a stream of data. The serialized data is then pre-emphasized and transmitted to the receiver through a bandwidth-limited channel. The receiver equalizes the received signal in order to compensate the high frequency spectrum loss before extracting the clock and data in the Clock and Data Recovery (CDR) loop.

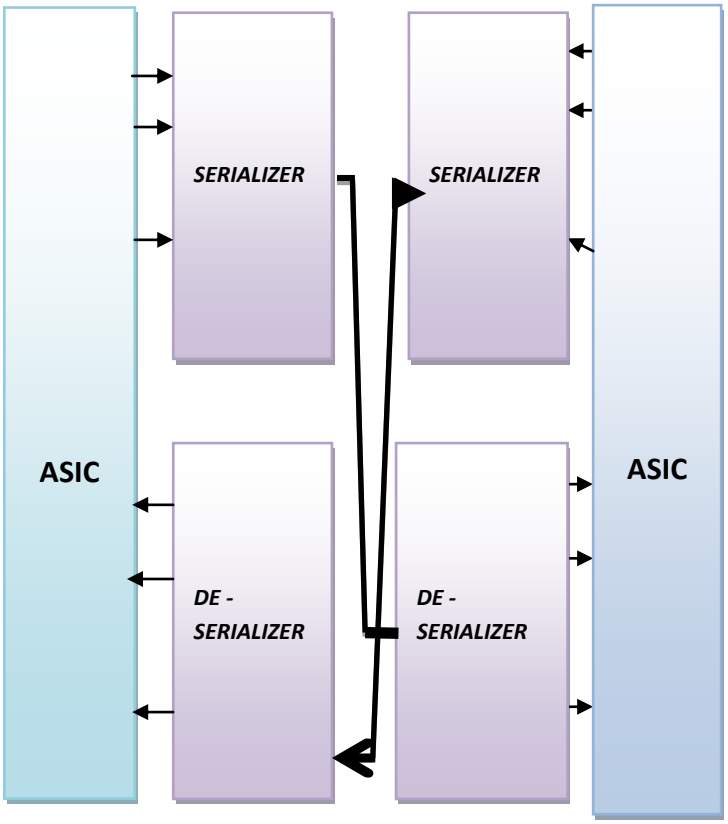

Fig 2. Data Serialize – De-Serialize ASIC CORE

TEXT Description: The above Diagram represents Data Serialize – De-Serialize ASIC. It Consists two IP cores on the left side Data Serialize converts parallel data into serial data format and the same serial data convert to parallel format on De-serialize side and vice versa. The goal of serialize the data is for save the process time multiple data packets and High speed serial communication at various high frequency standards.

II. Ultra High Frequency General and PRBS Data Serialize De-Serialize ASIC Architectures

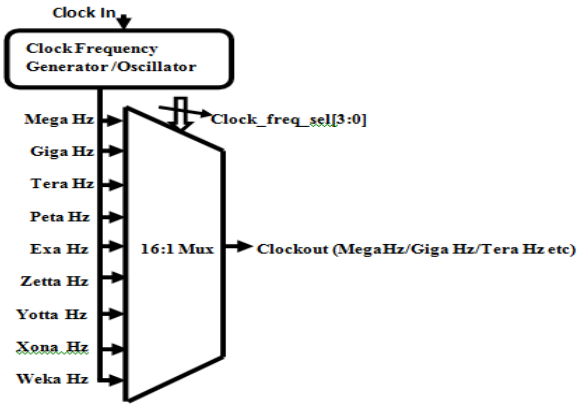

Fig.1: Multi Clock Frequency Generator

Description—Multi Clock Frequency Generator consists Clock Frequency Generator/Oscillator, 8:1 Multiplexer. Clock Frequency Generator . Generator consists Counter to Generates Different Clock Frequencies, MHz, GHz, THz, PHz, EHz, ZHz,YHz,XHz,WHz of 10^6 or 2^{20}, 10^9 or 2^{30}, 10^{12} or 2^{40}, 10^{15} or 2^{50} ,10^{18}or 2^{60} ,10^{21}or 2^{70}, 10^{24}or 2^{80}, 10^{27}or 2^{90} , 10^{30}or 2^{100} Clock Cycles. 9:1 Multiplexer Selects The one the above

frequencies to generate Baud Rate of Specific Clock. These frequencies are act as a clock input to the PRBS Receiver Design of Different Tapped Pattern Sequences.

[a] Ultra High Frequency (Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock) 32,64,128,256 bit Data Serialize and De-Serialize ASIC /SOC Array Architecture Block

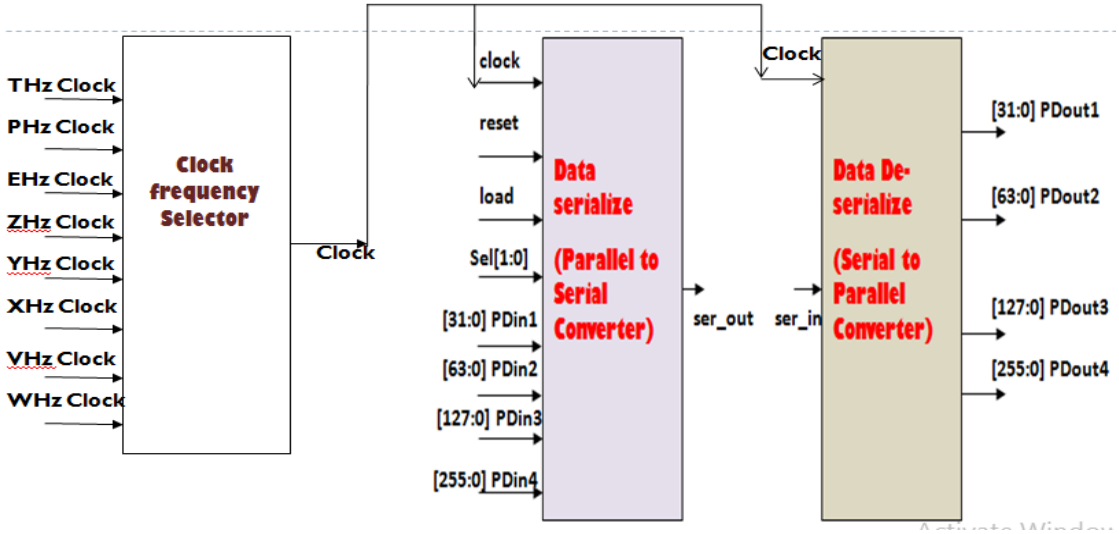

Fig.3 Ultra High Frequency Data Serialize De-Serialize ASIC/SOC Array

Description: The above diagram represents Ultra High Frequency Speed Tera, Peta, Exa, Zetta, Yotta, Xona, and Weka Hertz Clock Frequency Synchronized high speed baud rate (Tera bits per second(t.b.p.s), Peta bits per second(p.b.p.s), exa bits per second(e.b.p.s, zetta bits per second(z.b.p.s), Yotta bits per second, xona bits, weka bits per second(w.b.p.s)32,64,128,256 bit data width Data Serialize De- serialize ASIC IP Core. It consists of Data Serialize and De serialize ASIC IP core and ultra high frequency Clock generators (Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock). The Data Serialize consists of Parallel Data to Serial Data Conversion of different Parallel data Input bit widths 32,64,128,256 bits and the same serial data input De-serialize and convert form serial to parallel data output bit widths of 32,64,128,256 bits. These data Serialize and De-serialize are purely synchronized with Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock frequencies generated of Tera, Peta, Exa, Zetta,Yotta, Xona, Weka Hertz Clock Generators using frequency selector. The Tera Hertz, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock Generators consists of 40 bit, 50 bit, 60 bit, 70 bit, 80 bit, 90 bit, 100 bit Counters. One Tera Hertz Clock Cycle equal to 2^{40} Clock Cycles generated by 40 bit counter, it means $2^{40}/2$ clock cycles low period and $2^{40}/2$ clock cycles high period similarly for Peta Hertz Clock cycle equal to 2^{50} Clock Cycles generated by 50 bit counter, Exa Hertz Clock cycle equal to 2^{60} Clock Cycles generated by 60 bit counter, Zetta Hertz Clock cycle equal to 2^{70} Clock Cycles generated by 70 bit counter, Yotta Hertz Clock cycle equal to 2^{80} Clock Cycles generated by 80 bit counter, Xona Hertz Clock Cycle equal to 2^{90} Clock Cycles generated by 90 bit counter, Weka Hertz Clock cycle equal to 2^{100} Clock Cycles generated by 100 bit counter. The above data serialize de-serialize purely synchronize with these ultra high frequency clock cycle generators generates high speed data transfer baud rate in terms of t.b.p.s,p.b.p.s,e.b.p.s,z.b.p.s,y.b.p.s,x.b.p.s,w.b.p.s.

[b] Ultra High Frequency (Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock) Multichannel /Data port 32, 64,128,256 bit Data Serialize and De-Serialize ASIC /SOC Array RTL DUT

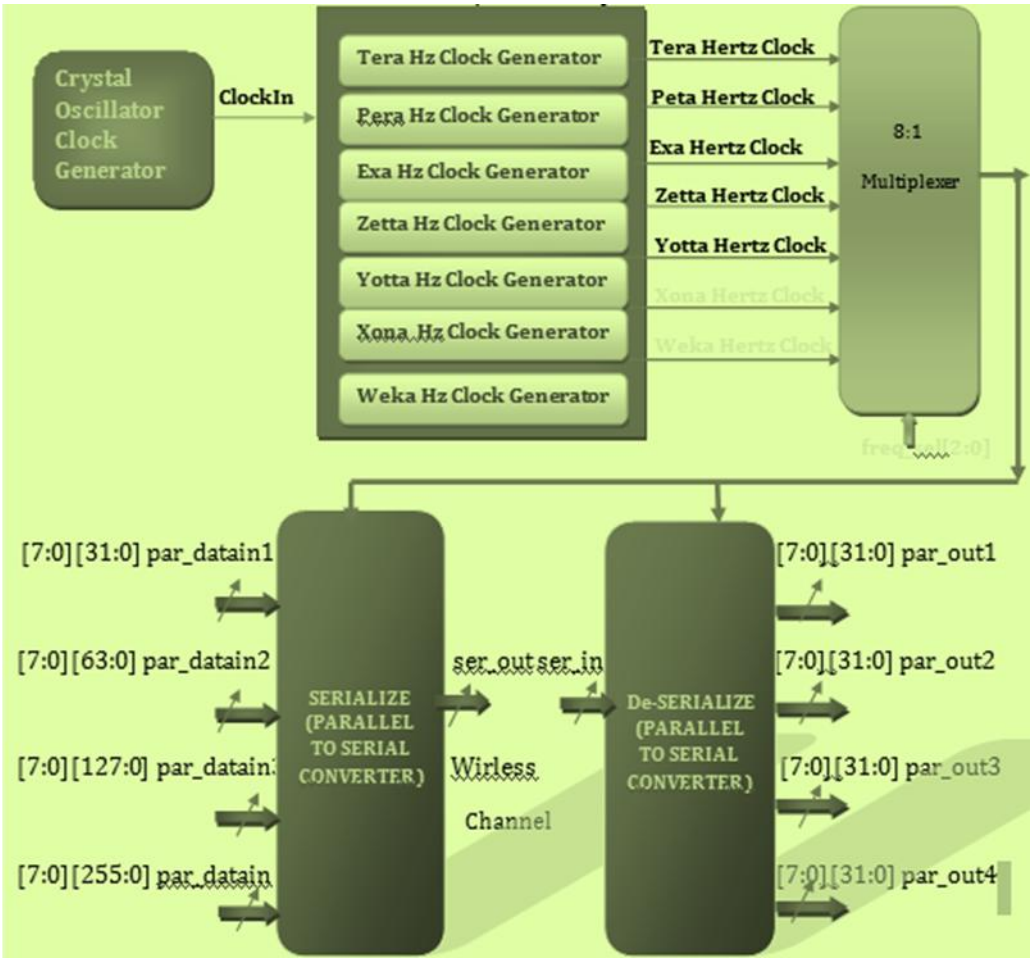

Fig.3 Ultra High Frequency Data Serialize De-Serialize Multichannel RTL DUT

The above diagram represents Ultra High Frequency Speed Tera, Peta, Exa, Zetta, Yotta, Xona, and Weka Hertz Clock Frequency Synchronized high speed baud rate (Tera bits per second(t.b.p.s), Peta bits per second(p.b.p.s), exa bits per second(e.b.p.s, zetta bits per second(z.b.p.s), Yotta bits per second, xona bits per second(y.b.p.s), weka bits per second(w.b.p.s) eight -32,64,128,256 bit data width 32 lane multichannel /data port multi dimension Data Serialize De- serialize ASIC IP Core. It consists of Data Serialize and De serialize ASIC IP core and ultra high frequency Clock generators (Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock). The Data Serialize consists of Parallel Data to Serial Data Conversion of different Parallel data Input bit widths 32,64,128,256 bits and the same serial data input De-serialize and convert form serial to parallel data output bit widths of eight 32,64,128,256 bits. These data Serialize and De-serialize are purely synchronized with Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock frequencies generated of Tera, Peta, Exa, Zetta,Yotta, Xona, Weka Hertz Clock Generators using frequency selector. The Tera Hertz, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Clock Generators consists of 40 bit, 50 bit, 60 bit, 70 bit, 80 bit, 90 bit, 100 bit Counters. One Tera Hertz Clock Cycle equal to 2^{40} Clock Cycles generated by 40 bit counter, it means $2^{40}/2$ clock cycles low period and $2^{40}/2$ clock cycles high period similarly for Peta Hertz Clock cycle equal to 2^{50} Clock Cycles generated by 50 bit counter, Exa Hertz Clock cycle equal to 2^{60} Clock Cycles generated by 60 bit counter, Zetta Hertz Clock cycle equal to 2^{70} Clock Cycles generated by 70 bit counter, Yotta Hertz Clock cycle equal to 2^{80} Clock Cycles generated by 80 bit counter, Xona Hertz Clock Cycle equal to 2^{90} Clock Cycles generated by 90 bit counter, Weka Hertz Clock cycle equal to 2^{100} Clock Cycles generated by 100 bit counter.

The above data serialize de-serialize purely synchronize with these ultra high frequency clock cycle generators generates high speed data transfer baud rate in terms of t.b.p.s,p.b.p.s,e.b.p.s,z.b.p.s,y.b.p.s,x.b.p.s,w.b.p.s.

[C] Pseudo Random binary sequence Data serialize De-serialize ASIC

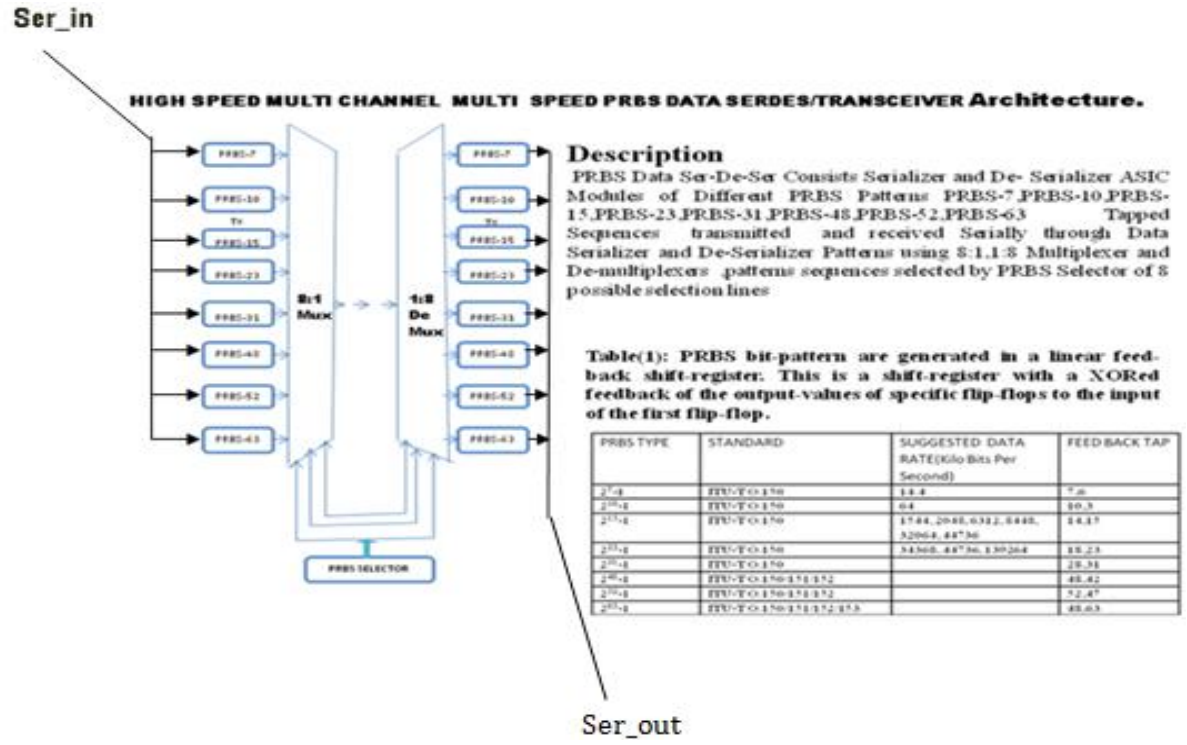

Fig.4 High speed multi channel multi speed PRBS Data SERDES

III. RESULTS SUMMARY

[a] Display results – 32,64,128,256 Data bit width Serialize De serialize

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Compiler version P-2019.06-1; Runtime version P-2019.06-1; Mar 21 08:53 2020
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Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
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Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxxxx01
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxxx010
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxx0101
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0

Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxxxx01010
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxxx010101
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxxx0101010
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxxx01010101
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxxx010101010
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxxxxx0101010100
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Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxxxx0101010100110
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Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxxx010101010011001
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxxx0101010100110011
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxxx01010101001100110
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxxxxxx01010101001100110101
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Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxxxx0101010100110011010101010
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 0
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxxx0101010100110011010101010101
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xxxxxxx0101010100110011010101010101
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
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Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:xx0101010100110011010101010011001
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1

Data De Serialize Serial in Parallel Data output1 PDout1:x01010101001100110101010100110011
Data Serialize Parallel in Serial out PDin1 = 55335533, ser_out1 = 1
Data De Serialize Serial in Parallel Data output1 PDout1:01010101001100110101010100110011

[b] Simulation Waveform Results -32,64,128,256 Data bit width Serialize De serialize SOC Core

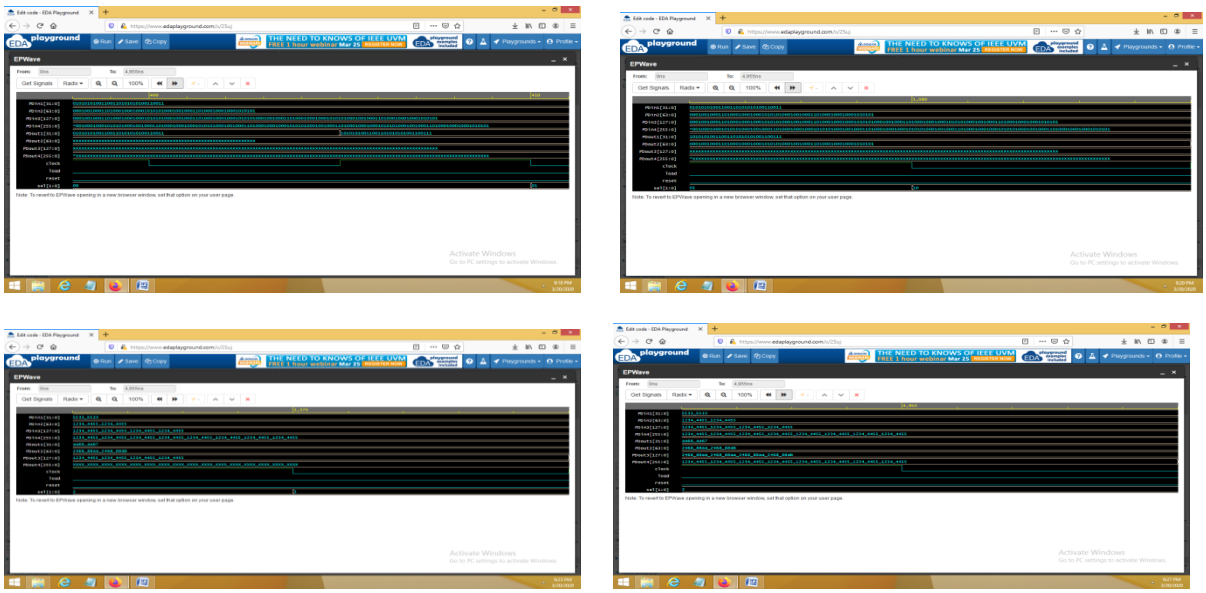

Fig.5 Simulation Wave form Results- General Data Serialize De-Serialize ASIC/SOC Core

[c] PRBS Data Serialize De- serialize Display Results

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Compiler version P-2019.06-1; Runtime version P-2019.06-1; Dec 7 07:43 2019
15prbs7 tapped seq ser_in = 1,ser_out = 1
25prbs7 tapped seq ser_in = 0,ser_out = 0
35prbs7 tapped seq ser_in = 1,ser_out = 1
45prbs7 tapped seq ser_in = 1,ser_out = 1
55prbs10 tapped seq ser_in = 0,ser_out = 0
65prbs10 tapped seq ser_in = 1,ser_out = 1
75prbs10 tapped seq ser_in = 0,ser_out = 0
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115prbs15 tapped seq ser_in = 1,ser_out = 1
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215prbs32 tapped seq ser_in = 0,ser_out = 0
255prbs48 tapped seq ser_in = 1,ser_out = 1
265prbs48 tapped seq ser_in = 0,ser_out = 0
305prbs52 tapped seq ser_in = 1,ser_out = 1
315prbs52 tapped seq ser_in = 0,ser_out = 0
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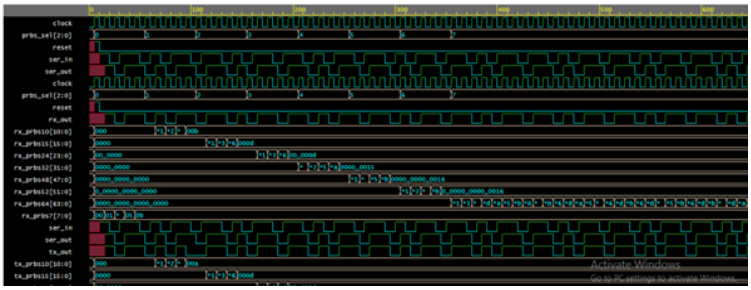

Fig.6 Simulation Wave form Results- Ultra high Frequency PRBS Data Serialize De-Serialize ASIC/SOC Core

IV. Conclusion

The idea is for We developed System Verilog /Verilog HDL RTL DUT & Test Bench Verification for ultra high frequency baud rate speed tera,peta, Exa,Zetta,Yotta,Xona,Weka Clock Frequency Synchronized 32,64,128,256 Data bit width Serialize De serialize SOC Core **width** using **FDSOI Technology** for Ultra high Speed long distance **6th sense space/satellite** Wireless Serialize De-serialize ASIC communication **Smart computing** products with leading EDA tools , this is newly invented product apart from existing data serialize de-serialize in terms frequency/speed, data transfer baud rate tera,peta ,exa, zetta bits per second , coverage with leading automation tool.

Prof. Executive Dean. P.N.V.M Sastry, et. al. "Ultra High Frequency Baud rate data transfer speed(Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Hertz Data T/s) General Data and PRBS Data Serialize De-Serialize ASIC /SOC Array card Design using FDSOI Technology for Ultra high Speed long distance 6th sense space/satellite Wireless communication Engineering Smart computing products/Applications." *IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)* 17(5), (2022): pp 53-62.